Abstracts

Interface Loss Mechanism of Millimeter-Wave Coplanar Waveguides on Silicon

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The interface loss mechanisms of coplanar waveguides (CPWs) on silicon with an SiO/sub 2/ isolation layer are investigated. The total losses of straight CPW lines of 7.5-mm length are measured between 45 MHz and 40 GHz and the interface contribution is extracted from that by its bias dependence. The interface losses depend on bias voltage and on the oxide quality. With an optimal bias voltage, the attenuation of a CPW with an unpatterned oxide layer always achieves a minimum. With bias between the flat-band voltage V/sub FB/ and threshold voltage V/sub T/ (depletion region), the interface losses are negligible. For high quality oxides (V/sub T/ around 0 V), very low attenuation was obtained without any bias.

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